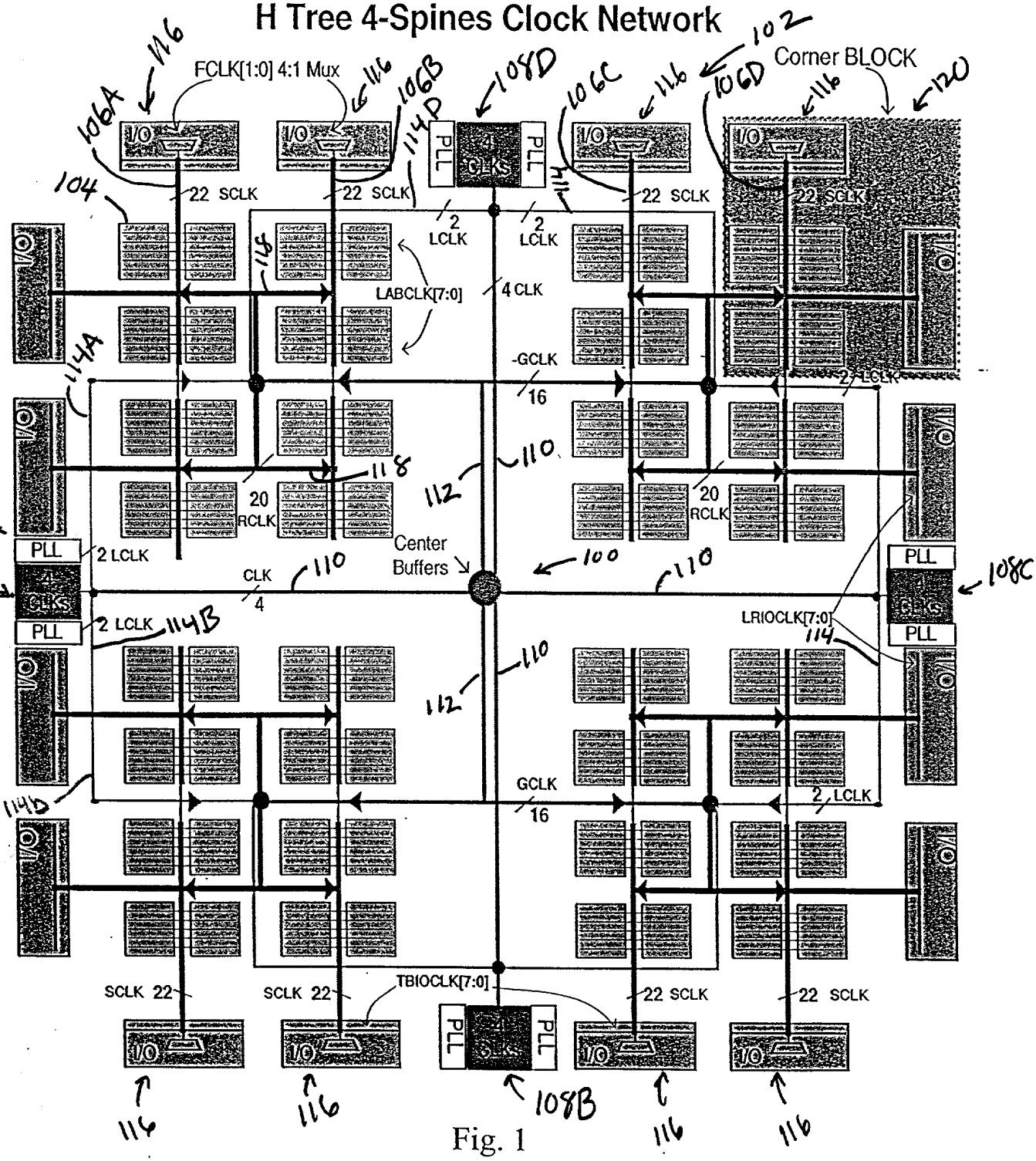
H Tree 4-Spines Clock Network
FCLK[1:0] 4:1 Mux
Corner BLOCK
22 SCLK
2 LCLK
LABCLK[7:0]
4 CLK
-GCLK
16
20 RCLK
Center Buffers
CLK
4
GCLK
LRIOCLK[7:0]
TBIOCLK[7:0]
PLL
4 CLKS
I/O
102
104
106A
106B
106C
106D
108A
108B
108C
108D
110
112
114A
114B
114C
114D
116
118
120

Fig. 1

H Tree 2-Spines Clock Network

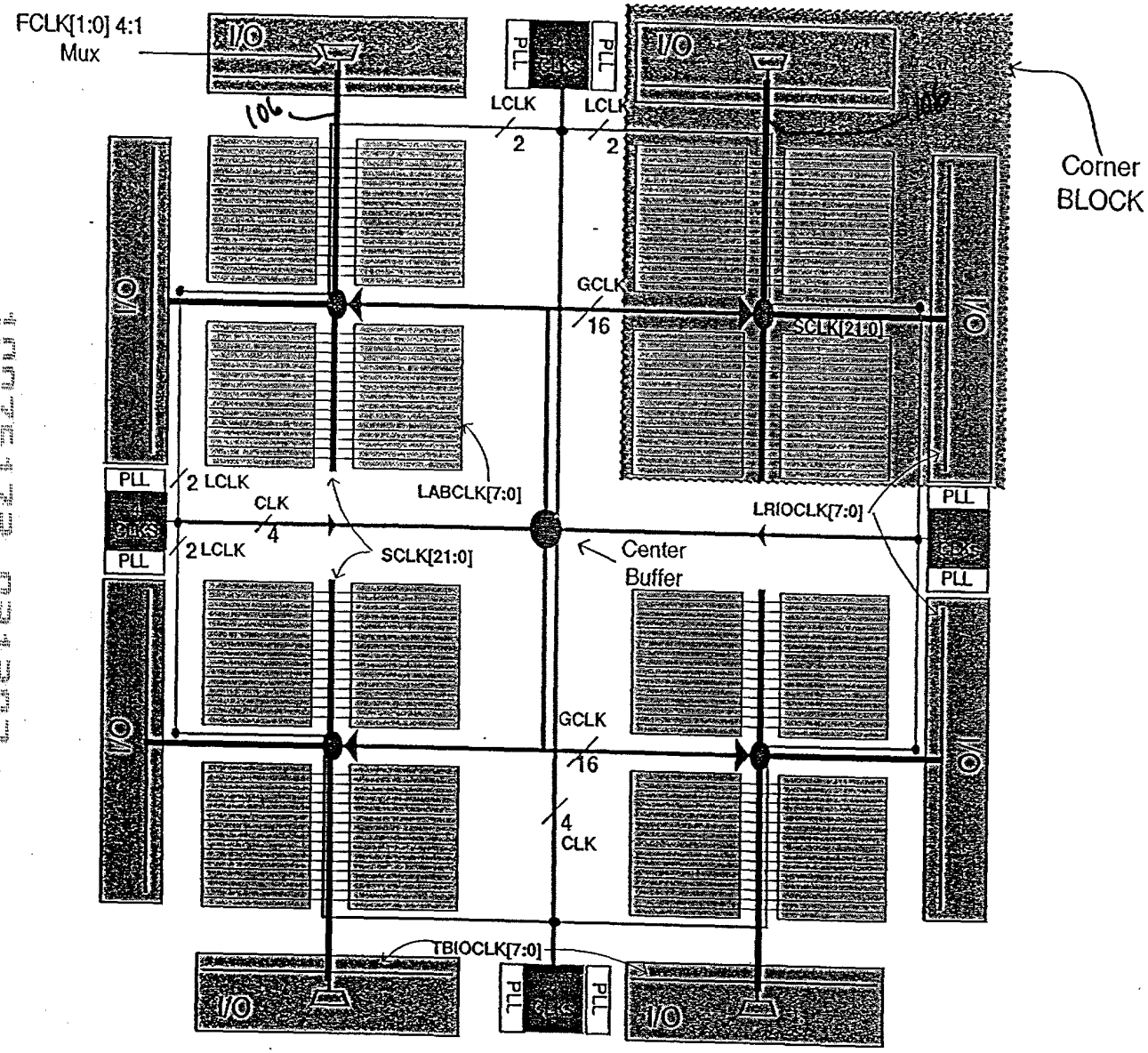

Fig. 2

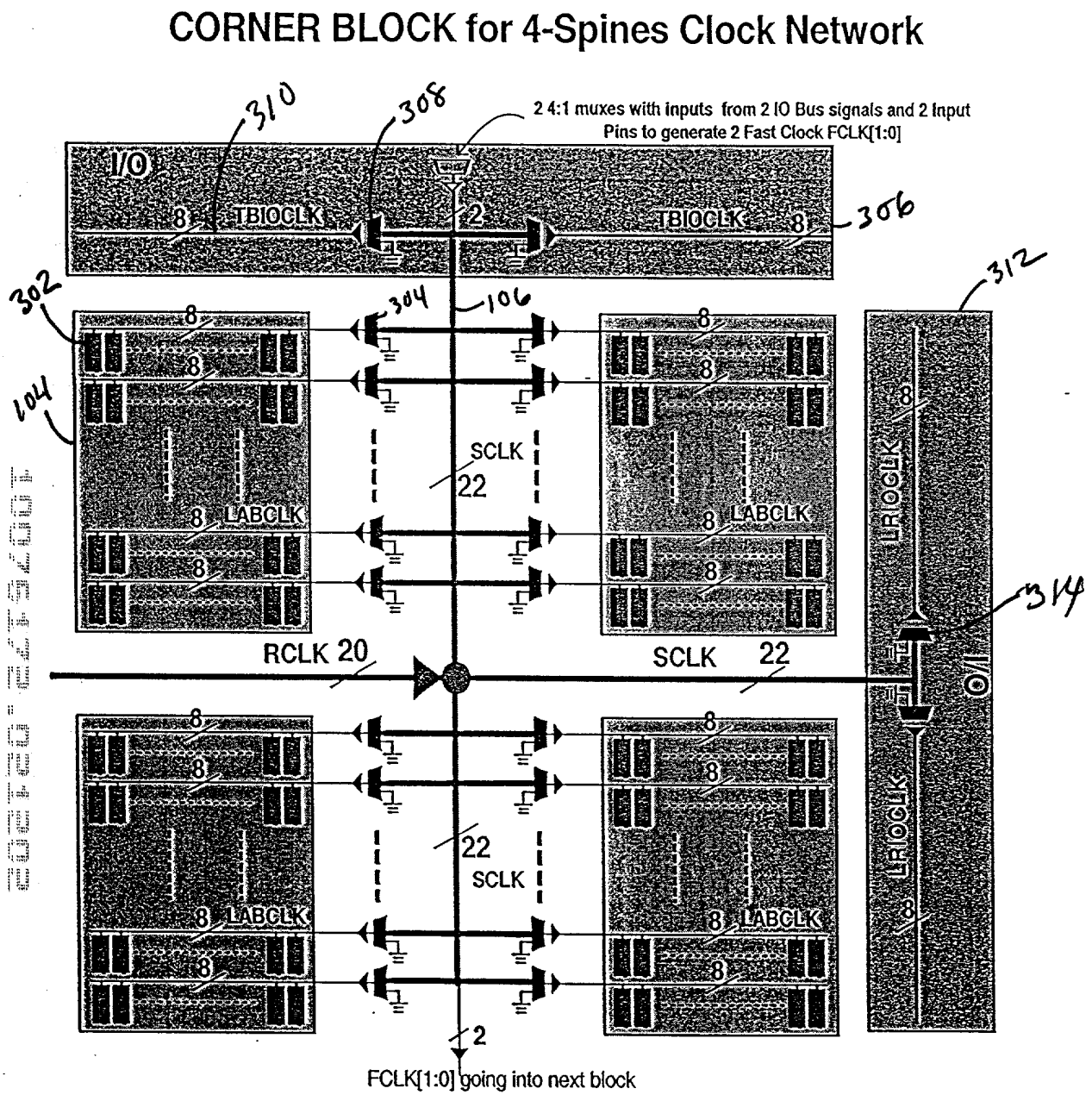
CORNER BLOCK for 4-Spines Clock Network
2 4:1 muxes with inputs from 2 IO Bus signals and 2 Input Pins to generate 2 Fast Clock FCLK[1:0]
310
308
306
302
304
106
104
312
314
I/O
TBIOCLK
LABCLK
SCLK
22
RCLK 20
LRIOCLK
FCLK[1:0] going into next block

Fig. 3

CORNER BLOCK for 2-Spines Clock Network

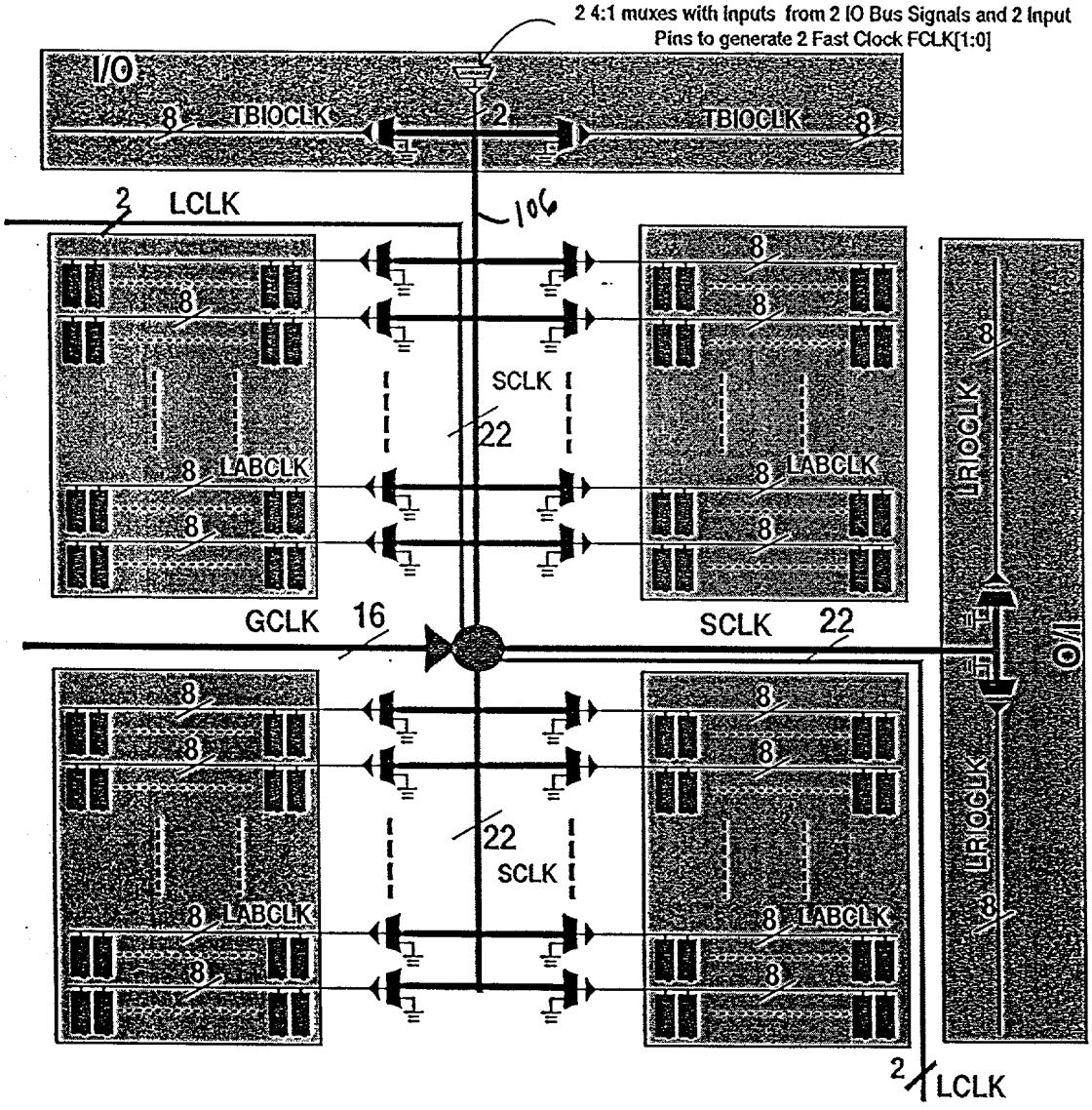

Fig. 4

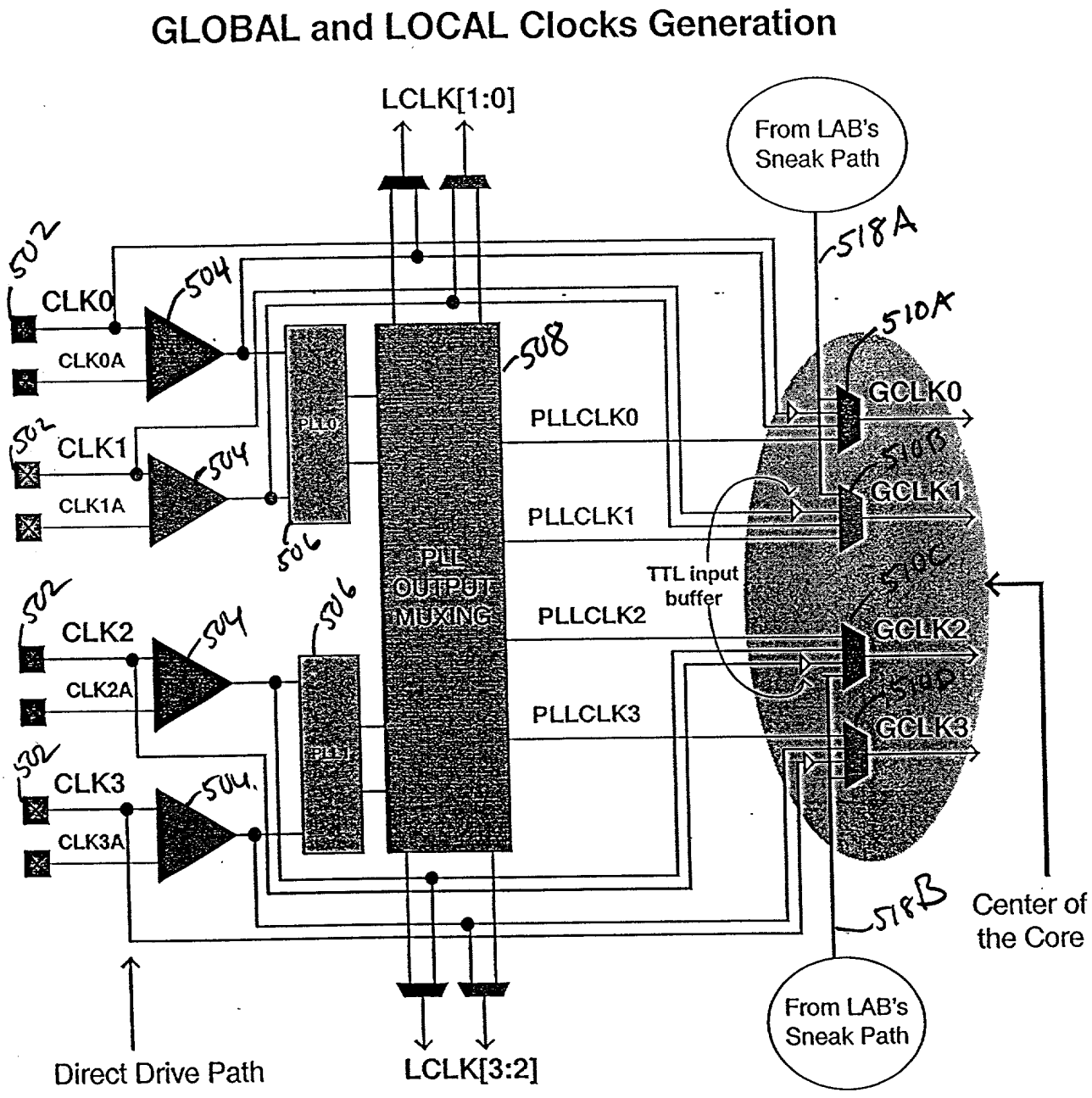
GLOBAL and LOCAL Clocks Generation
LCLK[1:0]
From LAB's Sneak Path
502
504
CLK0
CLK0A
CLK1
CLK1A
CLK2
CLK2A
CLK3
CLK3A
506
PLL0
PLL1
508
PLL OUTPUT MUXING
PLLCLK0
PLLCLK1
PLLCLK2
PLLCLK3
510A
510B
510C
510D
GCLK0
GCLK1
GCLK2
GCLK3
TTL input buffer
518A
518B
Center of the Core
From LAB's Sneak Path
Direct Drive Path
LCLK[3:2]

Fig. 5

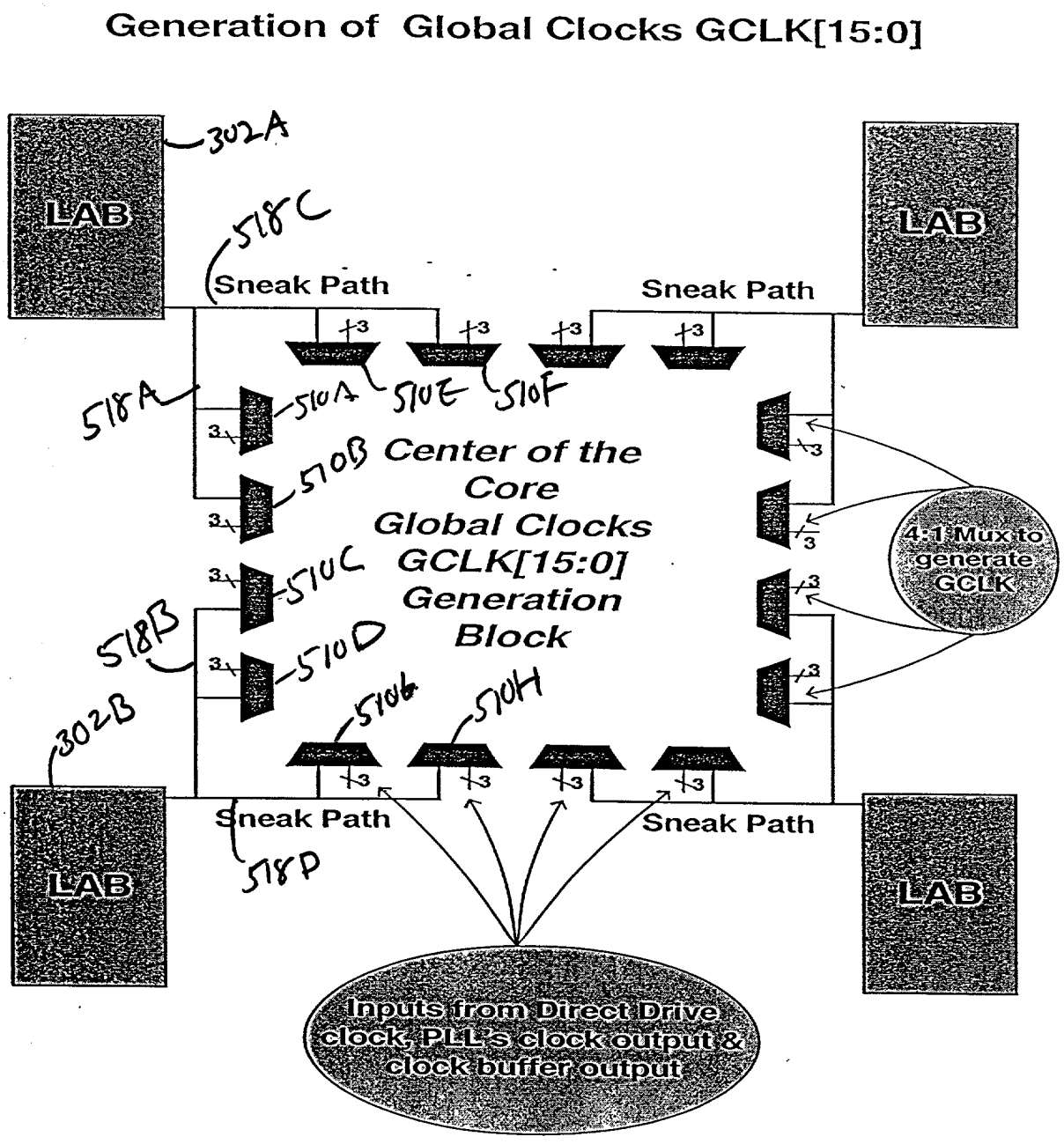
Generation of Global Clocks GCLK[15:0]
LAB
302A
518C
Sneak Path
Sneak Path
LAB
518A
510A
510E
510F
510B
Center of the Core
Global Clocks GCLK[15:0] Generation Block
510C
518B
510D
4:1 Mux to generate GCLK
302B
5106
510H
LAB
Sneak Path
518D
Sneak Path
LAB
Inputs from Direct Drive clock, PLL's clock output & clock buffer output

Fig. 6

Power Bus Segmentation for CLOCKs

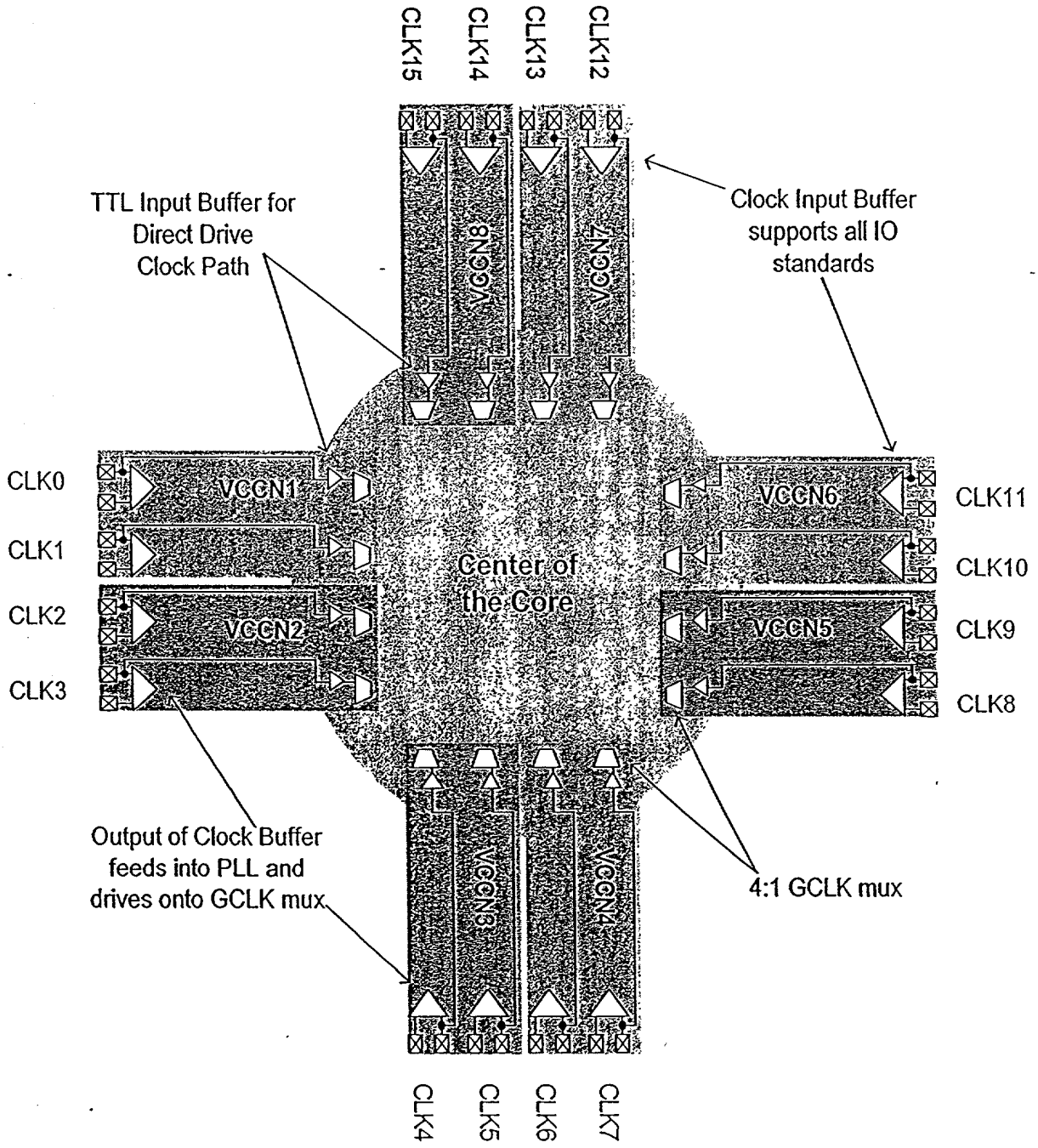

Fig. 7